ABSTRACT OF THE DISCLOSURE

In a synchronous multi-port bank memory, registers/buffers receive a read/write signal and an address signal from each of external ports, receive and send a data signal to and from each of the external ports, and receive and send a port block signal. An access conflict management circuit receives the address signals from the registers and buffers and generates the port block signal when an access conflict to the bank occurs. A switching network receives the read/write signal and the address signal from the registers/buffers and generates a bank selection signal when no port block signal is received, so as to activate the selected bank. Thus, memory access cycle time is shortened. A synchronous 1-port bank memory is also constructed similarly.